

Lois Orosa Nogueira

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Research Interests

Computer Architecture

Memory Systems, Hardware Security and Reliability, Data Centric Computing, New Memory Technologies, AI Hardware-Software Co-design, Storage Systems, Parallel Systems, Quantum Computing Reliability and Security.

Institutional Leadership

Scientific Director

Galicia Supercomputing Center (CESGA)

*Santiago de Compostela,
Spain
Sept 2025 – present*

- Scientific Director
- Designing a Scientific Strategy for scaling the institution
- Institutional representative
- Get and lead the European AI Factory 1HealthAI (82M EUR)

Managing Director

Galicia Supercomputing Center (CESGA)

*Santiago de Compostela,
Spain
Mar 2022 – Sept 2025*

- Leading CESGA's strategic change.– Contributing to attract large European Funds for infrastructure, services and research.
- CESGA Representative in the Galicia Quantum Technology Hub (2022-2030, 154M EUR)
- Quantum Computer with more Qubits in South Europe (2023, 32 Qubits, 14M EUR)
- Second largest Supercomputer in Spain (Finisterrae III, 2022, 7M EUR)

Education

University of Santiago de Compostela

in Computer Architecture

*Santiago de Compostela,
Spain
Dec 2008 – Sept 2013*

- Thesis: New Hardware Support for Transactional Memory and Parallel Debugging in Multicore Processors
- Advisor: Elisardo Antelo and Javier Bruguera
- Supported by the project "Hardware and software support for high performance computing" (TIN201017541)
- Interuniversity PhD Courses in Information Technology (University of Santiago de Compostela and University of A Coruña)

University of Vigo

M.Eng in Telecommunications Engineering

*Vigo, Spain
Sept 2000 – June 2006*

Academia

Senior Researcher

Galicia Supercomputing Center (CESGA)

*Santiago de Compostela,
Spain
Sept 2025 – present*

Design Reliable, secure and efficient computing systems for AI and other emerging applications

- Ramón y Cajal tenure track contract (ranked 1st with a score of 100/100)
- Leading a Consolidación Investigadora project (199.927 EUR.)
- Xunta the Galicia Consolidator Grant (115.000 EUR.)
- Leading the Experimental platform of the 1HealthAI AI Factory (4M EUR.)

Senior Researcher

ETH Zürich, D-ITET, SAFARI group
Memory Systems and Hardware Security

- PI: Onur Mutlu

Zurich, Switzerland
Jan 2019 – Mar 2022

PostDoctoral Fellow

University of Campinas (UNICAMP), LSC
Architectural Support for Speculative Program Execution

- Supported by FAPESP grant 2014/03840-2.
- PI: Rodolfo Azevedo.

Campinas, Brazil
June 2014 – July 2018

Academic Guest

ETH Zürich, Department of Computer Science, SAFARI Group
Enabling security features in commodity DRAM chips

- Supported by FAPESP grant 2016/18929-4.
- Supervisor: Onur Mutlu

Zürich, Switzerland
Jan 2017 – Dec 2017

PostDoctoral Researcher

University of Santiago de Compostela

- Supervisor: Elisardo Antelo and Javier Bruguera

Santiago de Compostela,
Spain
Jan 2014 – May 2014

PostDoctoral Researcher

Universidade Nova de Lisboa
Hardware support for detecting atomicity violations.

- Supported by European Cooperation in Science and Technology (COST) with a Short-term Scientific Mission (STSM).
- Supervisor: João Lourenço

Lisboa, Portugal
Sept 2013 – Dec 2013

Scholarship

University of Illinois at Urbana-Champaign (UIUC), U.S.A.
Tolerating concurrency bugs in multicore processors

- Department of Computer Science, IACOMA group
- Advisor: Josep Torrellas

Urbana-Champaign, U.S.A
Sept 2009 – Dec 2009

Industry Experience

Internship

Xilinx Research
Training Convolutional Neural Networks (CNNs)

- Mentors: Michaela Blott, Yaman Umuroglu

Dublin, Ireland
July 2018 – Dec 2018

Internship

Recore Systems
Development of a shared memory multicore simulator.

- Mentor: Gerard Rauwerda

Dublin, Ireland
Aug 2012 – Dec 2012

Summer Internship

IBM R&D Labs
Development of compiler-based deterministic replay for X10 Language

- Mentors: Olga Golovanevsky, Marina Biberstein, Bilha Mendelson

Dublin, Ireland
July 2010 – Nov 2010

R&D Engineer
Arantia 2010 (Televes Group)

Santiago de Compostela,
Spain
2006

Development of network multimedia applications (TV streaming, multimedia contents).

Engineer
Communitel Global S.A (Vodafone)

Vigo, Spain
Apr 2006 – Oct 2006

Resolve second level maintenance issues, and automatize large-scale production tasks with perl and C.

Engineer
Communitel Global S.A (Vodafone)

Vigo, Spain
July 2005 – Oct 2005

Development of a web-based application for monitoring and controlling the network infrastructure.

Publications

"**SpyHammer: Understanding and exploiting RowHammer under fine-grained temperature variations**", Orosa, Lois, Ruhmair, Ulrich, Yaglikci, A Giray, Luo, Haocong, Olgun, Ataberk, Jattke, Patrick, Patel, Minesh, Kim, Jeremie S, Razavi, Kaveh, Mutlu, Onur, *IEEE access*. [PDF](#) ACCESS'24

"**DRAM bender: An extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM chips**", Olgun, Ataberk, Hassan, Hasan, Yaglikci, A Giray, Tugrul, Yahya Can, Orosa, Lois, Luo, Haocong, Patel, Minesh, Ergin, Oguz, Mutlu, Onur, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD'23)*. [PDF](#) TCAD'23

"**Alp: Alleviating cpu-memory data movement overheads in memory-centric systems**", Ghiasi, Nika Mansouri, Vijaykumar, Nandita, Oliveira, Geraldo F, Orosa, Lois, Fernandez, Ivan, Sadrosadati, Mohammad, Kanellopoulos, Konstantinos, Hajinazar, Nastaran, Luna, Juan Gomez, Mutlu, Onur, *IEEE Transactions on Emerging Topics in Computing (TETC'22)*. [PDF](#) TETC'22

"**EcoFlow: Efficient Convolutional Dataflows on Low-Power Neural Network Accelerators**", Orosa, Lois, Koppula, Skanda, Kanellopoulos, Konstantinos, Umuroglu, Yaman, Kanellopoulos, Konstantinos, Gomez-Luna, Juan, Blott, Michaela, Vissers, Kees, Mutlu, Onur, *IEEE Transactions on Computers (TC'23)*. [PDF](#) TC'23

"**Understanding Rowhammer under Reduced Wordline Voltage: An experimental study using real dram devices**", Yaglikci, A Giray, Luo, Haocong, De Oliviera, Geraldo F, Olgun, Ataberk, Patel, Minesh, Park, Jisung, Hassan, Hasan, Kim, Jeremie S, Orosa, Lois, Mutlu, Onur, *52nd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN'22)*. [PDF](#) DSN'22

"**pLUTo: Enabling Massively Parallel Computation in DRAM via Lookup Tables**", Ferreira, Joao Dinis, Falcao, Gabriel, Gomez-Luna, Juan, Alser, Mohammed, Orosa, Lois, Sadrosadati, Mohammad, Kim, Jeremie S, Oliveira, Geraldo F, Shahroodi, Taha, Nori, Anant, Mutlu, Onur, *55th IEEE/ACM International Symposium on Microarchitecture (MICRO'22)*. [PDF](#) MICRO'22

"**Hira: Hidden Row Activation for Reducing Refresh Latency of Off-The DRAM Chips**", Yaglikci, A Giray, Olgun, Ataberk, Patel, Minesh, Luo, Haocong, Hassan, Hasan, Orosa, Lois, Mutlu, Onur, *55th IEEE/ACM International Symposium on Microarchitecture (MICRO'22)*. [PDF](#) MICRO'22

- "**NEON: Enabling Efficient Support for Nonlinear Operations in Resistive RAM-based Neural Network Accelerators**", Manglik, Aditya, Patel, Minesh, Mao, Haiyu, Salami, Behzad, Park, Jisung, Orosa, Lois, Mutlu, Onur, *arXiv preprint arXiv:2211.05730*. [PDF](#) arXiv'22
- "**Optically Connected Memory for Disaggregated Data Centers**", Gonzalez, Jorge, Palma, Mauricio G, Hattink, Maarten, Rubio-Noriega, Ruth, Orosa, Lois, Mutlu, Onur, Bergman, Keren, Azevedo, Rodolfo, *Journal of Parallel and Distributed Computing (JPDC'22)*. [PDF](#) JPDC'22
- "**DR-STraNGe: End-to-end System Design for DRAM-based True Random Number Generators**", Bostanci, F Nisa, Olgun, Ataberk, Orosa, Lois, Yaglikci, A Giray, Kim, Jeremie S, Hassan, Hasan, Ergin, Oguz, Mutlu, Onur, *28th IEEE International Symposium on High-Performance Computer Architecture (HPCA'22)*. [PDF](#) HPCA'22
- "**IChannels: Exploiting Current Management Mechanisms to Create Covert Channels in Modern Processors**", Haj-Yahya, Jawad, Orosa, Lois, Kim, Jeremie S, Gomez-Luna, Juan, Yaglikci, A Giray, Alser, Mohammed, Puddu, Ivan, Mutlu, Onur, *48th IEEE International Symposium on Computer Architecture (ISCA'21)*. [PDF](#) ISCA'21
- "**A Deeper Look into RowHammer's sensitivities: Experimental analysis of real DRAM Chips and Implications on Future Attacks and Defenses**", Orosa, Lois, Yaglikci, Abdullah Giray, Luo, Haocong, Olgun, Ataberk, Park, Jisung, Hassan, Hasan, Patel, Minesh, Kim, Jeremie S, Mutlu, Onur, *54th IEEE/ACM International Symposium on Microarchitecture (MICRO'21)*. [PDF](#) MICRO'21
- "**Reducing Solid-state Drive Read Latency by Optimizing Read-retry**", Park, Jisung, Kim, Myungsuk, Chun, Myoungjun, Orosa, Lois, Kim, Jihong, Mutlu, Onur, *26th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'21)*. [PDF](#) ASPLOS'21
- "**SynCron: Efficient Synchronization Support for Near-data-processing Architectures**", Giannoula, Christina, Vijaykumar, Nandita, Papadopoulou, Nikela, Karakostas, Vasileios, Fernandez, Ivan, Gomez-Luna, Juan, Orosa, Lois, Koziris, Nectarios, Goumas, Georgios, Mutlu, Onur, *27th IEEE International Symposium on High-Performance Computer Architecture (HPCA'21)*. [PDF](#) HPCA'21
- "**Blockhammer: Preventing rowhammer at low cost by blacklisting rapidly-accessed dram rows**", Yaglikci, A Giray, Patel, Minesh, Kim, Jeremie S, Azizi, Roknoddin, Olgun, Ataberk, Orosa, Lois, Hassan, Hasan, Park, Jisung, Kanellopoulos, Konstantinos, Shahroodi, Taha, Ghose, Saugata, Mutlu, Onur, *27th IEEE International Symposium on High-Performance Computer Architecture (HPCA'21)*. [PDF](#) HPCA'21
- "**DAMOV: A new methodology and benchmark suite for evaluating data movement bottlenecks**", Oliveira, Geraldo F, Gomez-Luna, Juan, Orosa, Lois, Ghose, Saugata, Vijaykumar, Nandita, Fernandez, Ivan, Sadrosadati, Mohammad, Mutlu, Onur, *IEEE Access*. [PDF](#) ACCESS'21
- "**Codic: A low-cost substrate for enabling custom in-dram functionalities and optimizations**", Orosa, Lois, Wang, Yaohua, Sadrosadati, Mohammad, Kim, Jeremie S, Patel, Minesh, Puddu, Ivan, Luo, Haocong, Razavi, Kaveh, Gomez-Luna, Juan, Hassan, Hasan, others, *48th IEEE International Symposium on Computer Architecture (ISCA'21)*. [PDF](#) ISCA'21

- "**FIGARO: Improving System Performance via Fine-grained in-DRAM Data Relocation and Caching**", Wang, Yaohua, Orosa, Lois, Peng, Xiangjun, Guo, Yang, Ghose, Saugata, Patel, Minesh, Kim, Jeremie S, Gomez-Luna, Juan, Sadrosadati, Mohammad, Ghiasi, Nika Mansouri, Mutlu, Onur, *53th IEEE/ACM International Symposium on Microarchitecture (MICRO'20)*. [PDF](#) MICRO'20
- "**Revisiting rowhammer: An Experimental Analysis of Modern DRAM Devices and Mitigation Techniques**", Kim, Jeremie S, Patel, Minesh, Yaglikci, A Giray, Hassan, Hasan, Azizi, Roknoddin, Orosa, Lois, Mutlu, Onur, *47th Annual International Symposium on Computer Architecture (ISCA'20)*. [PDF](#) ISCA'20
- "**FlexWatts: A Power-and Workload-aware Hybrid Power Delivery Network for Energy-efficient Microprocessors**", Haj-Yahya, Jawad, Alser, Mohammed, Kim, Jeremie S, Orosa, Lois, Rotem, Efraim, Mendelson, Avi, Chattopadhyay, Anupam, Mutlu, Onur, *53rd IEEE/ACM International Symposium on Microarchitecture (MICRO'20)*. [PDF](#) MICRO'20
- "**WoLFRaM: Enhancing Wear-leveling and Fault Tolerance in Resistive Memories using Programmable Address Decoders**", Yavits, Leonid, Orosa, Lois, Mahar, Suyash, Ferreira, Joao Dinis, Erez, Mattan, Ginosar, Ran, Mutlu, Onur, *38th IEEE International Conference on Computer Design (ICCD'20)*. [PDF](#) ICCD'20
- "**Evanesco: Architectural Support for Efficient Data Sanitization in Modern Flash-based Storage Systems**", Kim, Myungsook, Park, Jisung, Cho, Genhee, Kim, Yoona, Orosa, Lois, Mutlu, Onur, Kim, Jihong, *25th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'20)*. [PDF](#) ASPLOS'20
- "**Robust Machine Learning Systems: Challenges, Current Trends, Perspectives, and the Road Ahead**", Shafique, Muhammad, Naseer, Mahum, Theocharides, Theocharis, Kyrkou, Christos, Mutlu, Onur, Orosa, Lois, Choi, Jungwook, *IEEE Design & Test (D&T)*. [PDF](#) D&T'20
- "**CLR-DRAM: A Low-cost DRAM Architecture Enabling Dynamic Capacity-latency Trade-off**", Luo, Haocong, Shahroodi, Taha, Hassan, Hasan, Patel, Minesh, Yaglikci, A Giray, Orosa, Lois, Park, Jisung, Mutlu, Onur, *47th Annual International Symposium on Computer Architecture (ISCA'20)*. [PDF](#) ISCA'20
- "**Optically Connected Memory for Disaggregated Data Centers**", Gonzalez, Jorge, Gazman, Alexander, Hattink, Maarten, Palma, Mauricio G., Bahadori, Meisam, Rubio-Noriega, Ruth, Orosa, Lois, Glick, Madeleine, Mutlu, Onur, Bergman, Keren, Azevedo, Rodolfo, *32nd International Symposium on Computer Architecture and High Performance Computing*. [PDF](#) SBAC-PAD'20
- "**D-RaNGe: Using commodity DRAM Devices to Generate True Random Numbers with Low Latency and High Throughput**", Kim, Jeremie S, Patel, Minesh, Hassan, Hasan, Orosa, Lois, Mutlu, Onur, *5th IEEE International Symposium on High-Performance Computer Architecture (HPCA'19)*. [PDF](#) HPCA'19
- "**ITAP: Idle-time-aware Power Management for GPU Execution Units**", Sadrosadati, Mohammad, Ehsani, Seyed Borna, Falahati, Hajar, Ausavarungnirum, Rachata, Tavakkol, Arash, Abaee, Mojtaba, Orosa, Lois, Wang, Yaohua, Sarbazi-Azad, Hamid, Mutlu, Onur, *ACM Transactions on Architecture and Code Optimization (TACO)*. [PDF](#) TACO'19

- "**EDEN: Enabling Energy-efficient, High-performance Deep Neural Network Inference using Approximate DRAM**", Koppula, Skanda, Orosa, Lois, Yaglikci, A Giray, Azizi, Roknoddin, Shahroodi, Taha, Kanellopoulos, Konstantinos, Mutlu, Onur, *52nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'19)*. [PDF](#) MICRO'19
- "**Reducing DRAM Latency via Charge-level-aware Look-ahead partial Restoration**", Wang, Yaohua, Tavakkol, Arash, Orosa, Lois, Ghose, Saugata, Ghiasi, Nika Mansouri, Patel, Minesh, Kim, Jeremie S, Hassan, Hasan, Sadrosadati, Mohammad, Mutlu, Onur, *51st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'18)*. [PDF](#) MICRO'18
- "**AVPP: Address-first Value-next Predictor with Value Prefetching for Improving the Efficiency of Load Value Prediction**", Orosa, Lois, Azevedo, Rodolfo, Mutlu, Onur, *ACM Transactions on Architecture and Code Optimization (TACO)*. [PDF](#) TACO'18
- "**FLIN: Enabling Fairness and Enhancing Performance in Modern NVMe Solid State Drives**", Tavakkol, Arash, Sadrosadati, Mohammad, Ghose, Saugata, Kim, Jeremie, Luo, Yixin, Wang, Yaohua, Ghiasi, Nika Mansouri, Orosa, Lois, Gomez-Luna, Juan, Mutlu, Onur, *45th International Symposium on Computer Architecture (ISCA'18)*. [PDF](#) ISCA'18
- "**Asymmetric Allocation in a Shared Flexible Signature Module for Multicore Processors**", Orosa, Lois, Bruguera, Javier D, Antelo, Elisardo, *The Computer Journal (CJ'16)*. [PDF](#) CJ'16
- "**A Hardware Approach to Detect, Expose and Tolerate High Level Data Races**", Orosa, Lois, Lourenco, Joao, *4th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP'16)*. [PDF](#) PDP'16
- "**Temporal frequent value locality**", Orosa, Lois, Azevedo, Rodolfo, *3rd IEEE International Conference on Electronics, Circuits and Systems (ICECS'16)*. [PDF](#) ICECS'16
- "**Architecting a Computer with a Full Optical RAM**", Gonzalez, Jorge, Orosa, Lois, Azevedo, Rodolfo, *3rd IEEE International Conference on Electronics, Circuits and Systems (ICECS'16)*. [PDF](#) ICECS'16
- "**Flexsig: Implementing Flexible Hardware Signatures**", Orosa, Lois, Antelo, Elisardo, Bruguera, Javier D, *ACM Transactions on Architecture and Code Optimization (TACO)*. [PDF](#) TACO'12
- "**Pacman: Tolerating Asymmetric Data Races with Unintrusive Hardware**", Qi, Shanxiang, Otsuki, Norimasa, Nogueira, Lois Orosa, Muzahid, Abdullah, Torrellas, Josep, *8th International Symposium on High Performance Computer Architecture (HPCA'12)*. [PDF](#) HPCA'12

Workshops

- "**LogSI-HTM: Log Based Snapshot Isolation in Hardware Transactional Memory**", Orosa, Lois, Azevedo, Rodolfo, *7th Workshop on the Theory of Transactional Memory (WTTM'15)*. WTTM'15
- "**A Hardware Approach for Detecting, Exposing and Tolerating High Level Atomicity Violations**", Orosa, Lois, Lourenco, Joao, *Workshop on Dependable Multi-core and Transactional Memory Systems (DMTM'14)*. DMTM'14

Book Chapters

"*Using Approximate DRAM for Enabling Energy-Efficient, High-Performance Deep Neural Network Inference*", Orosa, Lois, Koppula, Skanda, Kanellopoulos, Konstantinos, Yaglikci, A Giray, Mutlu, Onur, *Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing: Hardware Architectures*, chapter 10. Springer'23

Posters

"*CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations*", Orosa, Lois, Wang, Yaohua, Sadrosadati, Mohammad, Kim, Jeremie, Patel, Minesh, Puddu, Ivan, Luo, Haocong, Razavi, Kaveh, Gomez-Luna, Juan, Hassan, Hasan, Mansouri, Nika Ghiasi, Ghose, Saugata, Mutlu, Onur, *9th IEEE International Symposium on Computer Architecture (ISCA '22)*,. ISCA'22

"*Dataplant: A Low-Cost In-DRAM Value Generation Primitive for Enabling System Security Features*", Orosa, Lois, Wang, Yaohua, Puddu, Ivan, Sadrosadati, Mohammad, Hassan, Hasan, Tavakkol, Arash, Mansouri, Nika Ghiasi, Patel, Minesh, Kim, Jeremie, Gomez-Luna, Juan, Seshadri, Vivek, Azevedo, Rodolfo, Mutlu, Onur, *ETH Systems Group Industry Retreat*. Retreat'18

"*Improving GPU Power and Energy Efficiency*", Sadrosadati, Mohammad, Mirhosseini, Amirhossein, Ehsani, Seyed Borna, Ausavarungnirun, Rachata, Tavakkol, Arash, Falahati, Hajar, Orosa, Lois, Wang, Yaohua, Sarbazi-Azad, Hamid, Falsafi, Babak, Mutlu, Onur, *ETH Systems Group Industry Retreat*. Retreat'18

"*Processing-In-Memory Benchmark Suite and Analysis*", Gomez-Luna, Juan, Tavakkol, Arash, Boroumand, Amirali, Olivera, Geraldo F, Atamaner, Mert, Sadrosadati, Mohammad, Mansouri, Nika Ghiasi, Orosa, Lois, Mutlu, Onur, *ETH Systems Group Industry Retreat*. Retreat'18

"*A Case for an Amnesic DRAM Chip*", Orosa, Lois, Wang, Yaohua, Sadrosadati, Mohammad, Hassan, Hasan, Tavakkol, Arash, Patel, Minesh, Seshadri, Vivek, Azevedo, Rodolfo, Mutlu, Onur, *ETH Industry day*. Industry'17

"*AVPP: Address-first Value-next Predictor with Value Prefetching*", Orosa, Lois, Azevedo, Rodolfo, Mutlu, Onur, *ETH Systems Group Industry Retreat*. Retreat'17

"*FlexSig: Implementing Flexible Hardware Signatures*", Orosa, Lois, Antelo, Elisardo, Bruguera, Javier D, *7th HiPEAC Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'12)*,. HiPEAC'12

(Invited) Research Talks

"*Computer Architecture Research in the Galicia Supercomputing Center: Challenges and Opportunities*", Orosa, Lois, *1st SAFARI Conference*. [Video](#) December 15th, 2025

"*CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations*", Orosa, Lois, *SAFARI Seminar, Global Online event*. [Video](#) February 10th, 2022

"*A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses*", Orosa, Lois, *SAFARI P&S SoftMC 2022 Spring Semester*. [Video](#) October 18th, 2022

- "*A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses*", Orosa, Lois, 54th IEEE International Symposium on Microarchitecture, Global Online event. October 21st, 2021
- "*CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations*", Orosa, Lois, 48th IEEE International Symposium on Computer Architecture, Global Online event. [Video](#) June 15th, 2021
- "*FIGARO: Improving System Performance via Fine-grained in-DRAM Data Relocation and Caching*", Orosa, Lois, 53rd IEEE/ACM International Symposium on Microarchitecture, Global Online event. [Video](#) October 19th, 2020
- "*More Capable and Efficient DRAM Main Memory Designs*", Orosa, Lois, Swiss Joint Research Center Workshop, École Polytechnique Fédérale de Lausanne (EPFL). January 30th, 2020
- "*EDEN: Enabling Energy-Efficient, High-Performance Deep Neural Network Inference Using Approximate DRAM*", Orosa, Lois, Computer Architecture Course (263-2210-00L), ETH Zurich. [Video](#) October 24th, 2019
- "*AVPP: Address-first Value-next Predictor with Value Prefetching for Improving the Efficiency of Load Value Prediction*", Orosa, Lois, 14th HiPEAC Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'19), Valencia, Spain. January 22nd, 2019
- "*ITAP: Idle-Time-Aware Power Management for GPU Execution Units*", Orosa, Lois, 14th HiPEAC Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'19), Valencia, Spain. January 23rd, 2019
- "*Temporal Frequent Value Locality*", Orosa, Lois, 27th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'16), London, England. July 6th, 2016
- "*Detecting, Exposing and Tolerating High Level Data Races*", Orosa, Lois, 2nd Manycore Workshop on Micro architectural Challenges in Performance, Energy Efficiency and Resilience, Campinas, Brazil. March 15th, 2016
- "*A Hardware Approach for Detecting, Exposing and Tolerating High Level Atomicity Violations*", Orosa, Lois, 24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP'16), Heraklion, Greece. February 19th, 2016
- "*Revisiting Load Value Speculation*", Orosa, Lois, Seminar series, University of Campinas, Brazil. April 17th, 2015
- "*Revisiting Load Value Speculation*", Orosa, Lois, Research Meeting: Performance, Energy and Reliability Challenges in Multi- and Many-core Platforms, Porto Alegre, Brazil. March 19th, 2015
- "*A Hardware Approach for Detecting, Exposing and Tolerating High Level Atomicity Violations*", Orosa, Lois, Workshop on Dependable Multicore and Transactional Memory Systems (DMTM), Vienna, Austria. January 22nd, 2014
- "*FlexSig: Implementing Flexible Hardware Signatures*", Orosa, Lois, 7th HiPEAC Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'12), Paris, France. January 23rd, 2012

"*A Cache Filtering Mechanism for Hardware Transactional Memory Systems Decoupled from Caches*", Orosa, Lois, *XX Jornadas de Paralelismo, A Coruña, Spain*. Jan 2009

"*Introduction to microprocessors and microcontrollers*", Orosa, Lois, *XCARFOS Summer course (Days of automatic control and robotics with open source tools)*. July 2009

Public Engagement and Institutional Impact (Incomplete)

"*Round table and talk: Galicia's Quantum Strategy, Projects and Infrastructures*", Orosa, Lois, *Italy-Spain bilateral Meeting on Quantum Technologies, Madrid (Italian Embassy and Blas Cabrera Institute)*. April 20-21, 2026

"*Talk: Centro de Supercomputación de Galicia (CESGA): Unha oportunidade para o ecosistema de I+D+i de Galicia*", Orosa, Lois, *TTick Talks (Atlantic, UVIGO)*. April 10, 2026

"*Talk: 1HealthAI: Factoría Europea de IA para Unha Soa Saúde*", Orosa, Lois, *Cátedra Camelia (CiTIUS)*. April 9, 2026

"*Talk: Centro de Supercomputación de Galicia (CESGA)*", Orosa, Lois, *Visit of Óscar López, Ministry of Digital Transformation of Spain*. April 9, 2026

"*Talk: 1HealthAI: a intelixencia artificial ao servizo da saúde, da biotecnoloxía e da transformación do coñecemento*", Orosa, Lois, *Acto de entrega dos Premios de Investigación en Saúde Transfronteiriza Galicia-Norte de Portugal (PISGA)*. February 4, 2026

"*Round Table: Infraestruturas e datos abertos (CESGA e DEUCALION)*", Orosa, Lois, *II Encontro Luso-Galaico de PLN, Santiago de Compostela*. March 13, 2026

"*O IGFAE e o CESGA impulsan o Quantum Computing Lab*", Orosa, Lois, *IGFAE (USC)*. [Web](#) January 14, 2026

"*La UVigo albergará un nuevo laboratorio de computación cuántica óptica de vanguardia (VQCC-CESGA Quantum Optical Computing Lab)*", Orosa, Lois, *Radio Vigo (Cadena SER)*. [Web](#) January 15, 2026

"*Interview: Lois Orosa, director del Cesga, sobre la nueva fábrica de IA: Va a ser una puerta a Europa*", Orosa, Lois, *Economía Digital Galicia*. [Web](#) December 23, 2025

"*Interview: Lois Orosa, director do CESGA: A factoría de IA é unha porta a Europa dende Santiago*", Orosa, Lois, *COPE Galicia*. [Web](#) October 23, 2025

"*¿Por qué la factoría europea de IA convertirá a Galicia en referente mundial en innovación en salud?*", Orosa, Lois, *La Voz de Galicia*. [Web](#) October 11, 2025

"*Galicia logra un hito histórico al poner en marcha la línea de comunicación cuántica más larga de España*", Orosa, Lois, *esRadio (Libertad Digital)*. [Web](#) October 9, 2025

"*Europa quiere ganar soberanía con la inteligencia artificial en Galicia con una fábrica pionera*", Orosa, Lois, *COPE (La Linterna)*. [Web](#) October 15, 2025

"*Así será la nueva sede del Cesga en A Sionlla: las obras arrancarán en octubre*", Orosa, Lois, *El Correo Gallego*. [Web](#) August 13, 2025

" <i>Galicia enciende el computador cuántico más potente de España</i> ", Orosa, Lois, <i>La Voz de Galicia</i> . Web	July 4, 2025
" <i>Qmio, el supercomputador cuántico que consolida la posición estratégica del I+D+i gallego</i> ", Orosa, Lois, <i>El Correo Gallego</i> . Web	May 26, 2025
" <i>El sector biotech gallego confía en el Cesga para acelerar el descubrimiento de fármacos</i> ", Orosa, Lois, <i>La Voz de Galicia</i> . Web	April 16, 2025
" <i>El ecosistema biotech gallego afianza su apuesta para que la computación de altas prestaciones del Cesga reduzca costes y acelere el descubrimiento de fármacos</i> ", Orosa, Lois, <i>Bioga</i> . Web	April 15, 2025
" <i>Lois Orosa en De 0 a 100: O maior valor do Cesga é o apoio á comunidade científica</i> ", Orosa, Lois, <i>La Voz de Asturias</i> . Web	December 5, 2024
" <i>Hablan las protagonistas del mural de Yoseba MP que une superabuelas y computación cuántica</i> ", Orosa, Lois, <i>La Voz de Galicia</i> . Web	November 30, 2024
" <i>La Xunta aprobará el lunes la licitación de la obra de la nueva sede del Cesga en A Sionlla</i> ", Orosa, Lois, <i>La Voz de Galicia</i> . Web	October 19, 2024
" <i>La Xunta asegura que la nueva sede del Centro de Supercomputación situará Galicia a la vanguardia en Europa</i> ", Orosa, Lois, <i>Galicia Press (Europa Press)</i> . Web	October 18, 2024
" <i>Jornada de Usuarios 2024</i> ", Orosa, Lois, <i>CESGA</i> . Web	June 6, 2024
" <i>CESGA, unha Infraestrutura na Vangarda da Computación Europea</i> ", Orosa, Lois, <i>Os luns no Ateneo, Santiago de Compostela</i> . Video	December 18, 2023
" <i>Galicia por Diante Fin de Semana</i> ", Orosa, Lois, López, Ignacio, <i>Regional radio (RTVG)</i> . Web	November 19, 2023
" <i>Talk: CESGA in the Quantum Computing Era</i> ", Orosa, Lois, <i>Corunna Innovate Summit, Coruña</i> .	October 27, 2023
" <i>Interview for Sois los primeros</i> ", Orosa, Lois, <i>esRadio</i> . Web	October 22, 2023
" <i>El Correo Gallego mesa redonda FUTURIBLES</i> ", Orosa, Lois, Alonso, Manuel Ángel, Otero, María Antonia, <i>El Correo Gallego, Santiago de Compostela</i> . Web	October 19, 2023
" <i>Interview for TVG</i> ", Orosa, Lois, <i>Galicia Regional Television (TVG)</i> . Web	October 14, 2023
" <i>Reportaxe TVG</i> ", Orosa, Lois, <i>Galicia Regional Television (TVG)</i> . Web	October 4, 2023
" <i>QMIO Report</i> ", Orosa, Lois, <i>CESGA</i> . Web	October 3, 2023
" <i>QMIO Premiere</i> ", Orosa, Lois, <i>CESGA</i> . Video	October 2, 2023
" <i>Galicia Quantum Technologies Hub: Presentation Act</i> ", Orosa, Lois, <i>Santiago de Compostela</i> . Video	July 15, 2022
" <i>Fujitsu-CESGA Collaboration Agreement</i> ", Orosa, Lois, <i>CESGA</i> . Video	April 21, 2023
" <i>Quantum Computing Report</i> ", Orosa, Lois, <i>GCiencia</i> . Web	March 20, 2023

" <i>Finisterrae III Report</i> ", Orosa, Lois, <i>El País</i> . Web	October 14, 2022
" <i>Interview: Finisterrae III</i> ", Orosa, Lois, Martell, Chema, <i>A Golpe de Bit (RTVE)</i> .	October 3, 2022
" <i>Finisterrae III Premiere</i> ", Orosa, Lois, <i>CESGA</i> .	May 20, 2022
" <i>Interview for Radio Galega</i> ", Orosa, Lois, <i>Galicia Regional Radio (RTVG)</i> . Web	March 10, 2022
" <i>El compostelano Lois Orosa será el nuevo director del Centro de Supercomputación de Galicia</i> ", Orosa, Lois, <i>El Correo Gallego</i> . Web	February 24, 2022

Projects

" <i>PI of the 1HealthAI Factory</i> ", , PI of the 1HealthAI Factory, granted to CESGA. 82.000.000 EUR.	2025
" <i>PI of the Experimental Platform (1HealthAI AI Factory)</i> ", , Build reliable, secure and efficient computer systems for AI, and building Quantum Computing systems. 4.000.000 EUR.	2025
" <i>IN607D 2025/12 - Axudas do Programa de Consolidación e Estructuración de Unidades de Investigación Competitivas</i> ", , PI of the project 'Memorias e sistemas de computación eficientes e seguros'. 115.000 EUR.	2025
" <i>CNS2024-154583 - Consolidación Investigadora</i> ", , PI of the project 'DRAM Security in High Performance Computing Systems'. 199.927 EUR.	2024
" <i>RYC2023-045785-I - Ramón y Cajal Tenure Track Contract</i> ", , Ranked 1st in Information and Communication Technologies area. Title: More Capable, Secure and Efficient DRAM Main Memory Designs and Computer Architectures. Score: 100/100. 251.800 EUR.	2023
" <i>Researcher - Memory System Design for AI/ML Accelerators & ML/AI Techniques for Memory System Design</i> ", , Task 2946.001, 1 year. 100.000 CHF.	2022
" <i>FAPESP 2016/18929-4 - Speculative Techniques for Reducing the Memory Bottleneck Problem</i> ", , ETH Zurich, Switzerland, 1 year. 68.735 CHF.	2016
" <i>FAPESP 2014/03840-2 - Architecture Support for Speculative Program Execution</i> ", , University of Campinas, Brazil, 3 years. 239.990 BRL.	2014
" <i>Euro-TM Short Term Scientific Mission</i> ", , Universidade Nova de Lisboa, Lisbon, Portugal, 3 months. 3.500 EUR.	2013
" <i>HiPEAC Industrial PhD Internship - Recore Systems</i> ", , Recore Systems, Enschede, Netherlands, 4 months. 5.000 EUR.	2012
" <i>HiPEAC Industrial PhD Internship - IBM Haifa</i> ", , IBM Haifa, Israel, 3 months. 5.000 EUR.	2010
" <i>Researcher - Hardware and software support for high performance computing (TIN2010-17541)</i> ", , 185.400 EUR.	2010

Honors and Awards

- "*Top Pick in Hardware and Embedded Security 2025*", Top Picks, The paper Revisiting RowHammer: An Experimental Analysis of Modern DRAM Devices and Mitigation Techniques, was awarded a Top Pick in Hardware and Embedded Security 2025. The Top Picks award recognizes the best of the best in hardware security from among all hardware security papers published in the last six years, across all top security (e.g., IEEE S&P, USENIX SEC), architecture (e.g., ISCA, ASPLOS), computer-aided design (e.g., ICCAD, DAC, DATE) and hardware security (CHES) venues. 2025
- "*RYC2023-045785-I, Ramon y Cajal Tenure Track Contract*", Ministry of Science of Spain, Ranked 1st in Information and Communication Technologies area. Title More Capable, Secure and Efficient DRAM Main Memory Designs and Computer Architectures. **Score 100/100**, 251.800 EUR 2023
- "*R3 Certificate (established researcher)*", Ministry of Science of Spain, Certificate given to researchers who have developed a level of independence. **Score 96/100**. 2023
- "*Intel Hardware Security Academic Award 2022*", Intel, The paper BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows was nominated as a finalist for the Intel Hardware Security Academic Award 2022 (one of 4 finalists out of 34 nominations) 2022
- "*18 HiPEAC paper awards*", HiPEAC, I received **18 HiPEAC paper awards since 2017**. The HiPEAC Paper Award aims to encourage HiPEAC members to publish their work at conferences in which Europe is not strongly represented. The award is given to a HiPEAC member who presents a full paper in one of the following list of conferences, ASPLOS, DAC, FCCM, HPCA, ISCA, MICRO, PLDI, POPL Since 2017

PhD Students

- Jorge Luis Gonzalez Reaño** *University of Campinas, Brazil*
Thesis: Photonics opportunities in modern computing systems *Jan 2014 – Dec 2021*
- Co-advised with Rodolfo Azevedo

Teaching Experience

- Teaching Assistant** *Zurich, Switzerland*
ETH Zurich *Sept 2017 – Dec 2021*
- 263-2210-00L
 - Computer Architecture [Fall'17, Fall'19, Fall'20, Fall'21]
 - 263-2211-00L
 - Seminar in Computer Architecture [Spring'19, Fall'19, Spring'20, Fall'20, Spring'21, Fall'21]
 - 252-0028-00L
 - Digital Design and Computer Architecture [Spring'19, Spring'20, Spring'21]
- Lecturer** *Campinas, Brazil*
Institute of Computing, University of Campinas *Jan 2016 – June 2016*
- MC102
 - Algorithms and Computer Programming (90h), Spring'16

Service

Program Committees

- The 40th ACM International Conference on Supercomputing (ICS 2026)
- The 54th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN 2024)
- The 53rd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN 2023)
- Sixth Workshop on Attacks and Solutions in Hardware Security (ASHES 2022), co-located with ACM CCS 2022
- Fifth Workshop on Attacks and Solutions in Hardware Security (ASHES 2021), co-located with ACM CCS 2021

Organizing Committees

- Quantum Information in Spain 2023 (ICE-8)

Reviewer

- Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) [2025, 2026]
- Transactions on Dependable and Secure Computing (TDSC) [2025]
- The Supercomputing Journal [2023]
- Transactions on Information Forensics & Security (TIFS) [2022]
- ACM Computing Surveys (CSUR) [2020]
- Transactions on Architecture and Code Optimization (TACO) [2020]
- IEEE MICRO [2019, 2020]
- Computers and Security [2019]
- Design, Automation and Test in Europe Conference (DATE) [2019]
- IEEE Transactions on Computers [2015, 2016, 2017, 2019, 2024]
- ERAD-SP [2018]
- Journal of Universal Computer Science [2018]

Member of the Board of Trustees

- Galtia Foundation for attracting high-level research talent (GALTIA) [2026]

Skills

Programming Languages

C/C++, assembly, Python, Perl, Java, VHDL, Latex

Tools

Intel Instrumentation Pin Tool, DRAM Bender, SoftMC, Git

Simulators

Simics, GEMS, gem5, QEMU, Ramulator, Bochs, ZSim, DRAMSim, McPath, Spice, DRAMPower

Languages

Galician

Native speaker

Spanish

Native speaker

English

Fluent

Portuguese

Professional working proficiency